REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated March 23, 2005.

By the present Amendment, the claims have been amended to clarify the invention and new claims 16 and 17 have been added to further define the invention.

Briefly, the invention defined by the present claims is directed to an improved arrangement for a semiconductor storage apparatus which facilitates more efficiently erasing data in a plurality of nonvolatile semiconductor memories. This is discussed, for example, beginning on page 16, lines 12, et seq. As noted there, the present invention has benefits not only with regard to the writing operation but also during the erasing operation. In particular, as noted on page 17, lines 3-9;

> "During the predetermined time period, an erase command in another of the flash memories 4 different from the flash memory 4 which is under the erase process. Thus, the plurality of flash memories 4 are erased in parallel. Accordingly, the operation speed for erasing data with respect to the whole semiconductor disk pack is increased."

Reconsideration and removal of the 35 USC §102 and §103 rejections of claims 1-15 based on the U.S. Patent No. 5,724,544, to Nishi is respectfully requested. By the present Amendment, independent claim 1 has been amended to specifically define the feature that:

> "Wherein, after said first erase command has been sent, said control module sends a second erase command to another of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent to initiate a second internal erase operation of data within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command."

Thus, not only are the first and second erasing commands sent to a different nonvolatile semiconductor memory, but the second erasing command is sent while the first nonvolatile semiconductor memory is still performing the first internal erase operation. It is respectfully submitted that this feature is completely lacking from Nishi.

More specifically, as noted in the Office Action, Nishi does, indeed, send first and second erase commands to first and second nonvolatile memories. For example, lines 12-31 of Nishi discloses a memory controller 208 which sends a first erase signal EE1 to an EEPROM 30 to erase data in the EEPROM before sending a write signal WR1. A memory controller 210 sends a second erase signal EE2 to an EEPROM 40 which erases data in that EEPROM before sending a write signal WR2. However, Nishi fails to teach or suggest that the second erase signal is sent to the second EEPROM 40 while the data erase operation of the EEPROM 30 is being carried out in response to the first erase signal EE1. Thus, Nishi fails to teach or suggest the feature found in the amended claim 1 concerning the interleaving of the erase operations for the two different nonvolatile memories.

Accordingly, it is respectfully submitted that the amended claim 1, and its dependent claims 2-15, clearly defines over the Nishi reference, and reconsideration and allowance of this amended claim is respectfully requested.

Reconsideration and allowance of the new independent claim 16 and its dependent claim 17 over Nishi is also respectfully requested. Similar to claim 1, claim 16 defines:

> wherein, after said first erase command has been sent, said control module sends a second erase command to an other of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data

> in said block units within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command.

Thus, again, an interleave erasing operation of two nonvolatile memories is defined which is completely lacking from Nishi. Accordingly, reconsideration and allowance of independent claim 16 and its dependent claim 17 is respectfully requested.

If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 566.32253CC8).

Respectfully submitted,
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